A Simple Practical Technique for Estimating the Junction Temperature and the Thermal Resistance of a GaAs HBT

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Abstract — **This paper shows a practical technique to find a good estimate of the junction temperature and the thermal resistance in a GaAs HBT. The technique is based on simple calculations from the physical dimensions of the HBT and the thermal material parameters, without using any specialized 3D thermal software or equipment for thermal measurements. This work should be of great value for the circuit designers, who want to have an easy practical way of including good thermal values into models for accurate circuit simulations. Two different HBT's have been used to evaluate the technique presented in this paper. Evaluation of the present technique is done by comparing the junction temperature obtained by measurements done at Caswell Technology, to the estimated junction temperature from the present technique. The present technique shows good agreement with these measurements.**

I. Introduction

The main points for the success of an active circuit design are reliable models for the components. For large signal transistor amplifiers the thermal behaviors must be accurately described. The transistors thermal resistance, R_{th}, is therefore of great importance, together with the DC and the frequency dependent parameters.

There are several ways to find the thermal resistance. A full 3D thermal simulation can be used, but this is both time consuming and complicated. Software that is capable of doing 3D thermal simulations is expensive and usually inaccessible for the common circuit designer. Another way of finding the thermal resistance is by measurements at different temperatures and then calculates the thermal resistance. Methods describing this are given by [1]-[3]. The main disadvantage of these methods is that they require equipment for doing temperature measurements.

The objective here is to develop a simple technique capable of estimating the junction temperature and the thermal resistance from the geometrical layout of the transistor. The present technique is evaluated by comparing the results with measurements of the junction temperature for two different GaAs HBT transistors. The measurement results in [1] are found by using the methods described in [1]-[3]. The GaAs HBT's were developed by Caswell Technology [4].

II. Technology And Software

The transistors chosen for this work are HBT's produced in InGaP/GaAs technology by Caswell Technology. Two transistors were chosen both having the emitter up configuration. The first is a 40 μm long single finger transistor. The second transistor consists of four 40 μm long fingers located side by side with a spacing of 50 μm.

The only software needed is a mathematical tool like MATLAB.

III. Thermal Resistance Estimation Technique

The main assumption in this technique is that the contribution to the junction temperature is dependent only on three separate phenomena - the thermal conduction of the substrate, the thermal conduction of the metal connecting the emitter to the via-holes, and the effects of the via-holes. These effects can be calculated separately.

In a power device the metal connecting to the emitter is usually the top level metal, which is also the thickest. The top level metal is usually separated from the substrate by a polyimide layer, and connected to a via through the substrate to the backside. The separation of thermal conduction in the substrate and the thermal conduction of the top level metal is valid, when the separating layer has a low thermal conductivity. The thermal conductivity of gold is more than a factor of 1000 greater than that of polyimide. A rule of thumb is that this technique is valid as long as the length of the metal lines, connecting the emitter to the via-holes, is less than 1000 times the thickness of the polyimide layer.

The top of the gold filled via-holes will have approximately the same temperature as the backside of the substrate. A simple approximation of the top surface zone with zero temperature increase created by the via-holes is therefore included.

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In this technique, it is only necessary to calculate the temperature at the substrate surface. It is also assumed that the backside of the substrate is connected to an ideal heat-sink.

A. Heat Transfer In The Substrate

The heat transfer in the substrate is described by the heat flow equation:

$$\bar{\nabla} \cdot k(T)\bar{\nabla}T(x,y,z) = -P(x,y,z) \qquad (1)$$

P is the power density, T is the temperature, and k is the thermal conductivity.

Equation (1) reduces to the Laplace's equation when assuming that the thermal conductivity is independent of the temperature. It will be shown below that this assumption is valid here. In [5] a solution is presented, and it is repeated here in Equation (2) for clarity. Equation (2) shows the temperature at a point (x, z) on the substrate surface calculated from a point source placed at the point (x_0, z_0).

$$T(x,z) = \frac{P_{GaAs}}{2\pi \cdot k_{GaAs}\sqrt{(x-x_0)^2 + (z-z_0)^2}} \qquad (2)$$

P_{GaAs} is the power dissipated into the GaAs substrate in W and k_{GaAs} is the thermal conductivity in W/cm/K at a constant temperature.

The transistor is assumed to be a flat rectangular plate heat source of length L and width W equal to the size of the emitter.

The temperature in any point on the substrate surface is then found by integrating Equation (2) over the rectangular heat source. This can easily be done in MATLAB by numerical integration.

The backside of the substrate is assumed to be connected to an ideal heat-sink. This is modeled by imaging the real heat source with an equivalent negative one placed below the backside at a distance equal to the substrate thickness. The overall temperature function at the substrate surface is a sum of the contribution from these two heat sources.

The contribution ($T_{j,GaAs}$) to the junction temperature (T_j) from the heat conduction in the substrate is then found by calculating the average temperature across the rectangular heat source.

B. Heat Transfer In The Top Level Metal

The heat transfer in the top-level metal can easily be calculated from Equation (3).

$$T_M = P_M \cdot R_{t,M} \qquad (3)$$

T_M is the temperature increase at the emitter in Kelvin, P_M is the heat flowing in the metal from the emitter to the via-holes in W. $R_{t,M}$ is the thermal resistance of the metal in K/W.

The thermal resistivity of a rectangular metal line is given by Equation (4):

$$R_{t,M} = \frac{L_m}{k_m W_m h_m} \qquad (4)$$

k_m is the thermal conductivity of the metal in W/cm/K, and L_m, W_m and h_m is the length width and height of the metal line in meter.

C. The Effects Of The Via-Holes

The vertical via-holes generate areas in the substrate where the temperature is practically equal to the ambient temperature of the backside of the substrate. To emulate the effect of a via-hole, the via-hole is replaced by a negative point source at the substrate surface level. The power and position of the negative point source is selected in such way that the total temperature increase in the substrate from the negative point source and the transistor, is zero along the edge of the via-hole. See Fig. 1. The via-hole itself is removed.

The contribution ($T_{j,Via}$) to the junction temperature (T_j) from the negative heat source in the via, is found by the average temperature contribution across the rectangular plate.

D. Junction Temperature And The Thermal Resistance

The total power dissipated in the transistor is flowing partly in the metal and partly in the substrate. The total dissipated power is divided in such a way that the temperature in the metal at the emitter is equal to the temperature in the substrate at the emitter, including the effect of the via-hole. Equation (5) describes this relation:

$$\left.\begin{aligned} P_{GaAs} &= nP_{tot} \\ P_M &= (1-n)P_{tot} \end{aligned}\right\} \Rightarrow T_M = T_j = T_{j,GaAs} + T_{j,Via} \qquad (5)$$

where the value of n is chosen to fulfill Equation (5).

The junction temperature, T_j, calculated here is only valid for a constant value of the thermal conductivity, k_{GaAs}, in the substrate. However, the thermal conductivity is dependent on the temperature, and the temperature changes with the distance fr0m the transistor. The

dependence of the thermal conductivity on temperature of GaAs is discussed in [6], and is shown to be:

$$k_{GaAs} = 745 \cdot T^{-1.30} \quad (6)$$

where T is in Kelvin, and k_{GaAs} is in W/cm/K.

The technique for estimating the junction temperature T_j, is to calculate T_j for two different thermal conductivities, which gives the upper and lower limits of T_j. The actual value of the T_j will be between these limits. The two thermal conductivities are found by choosing two temperatures, the ambient temperature and the maximum junction temperature, which covers the possible range of temperatures inside the device.

The thermal resistance of the transistor can be found by dividing the junction temperature by the total dissipated power, as shown in Equation (7).

$$R_{th} = \frac{T_j}{P_{tot}} \quad (7)$$

IV. Results And Discussion

The technique described in Section III is applied to the transistors in Section II. The results from the present technique are compared to the results obtained in [1]. In [1], 3D thermal simulations have been used to obtain the results for the single finger transistor. The result for the four-finger transistor is found in [1] from measurements using methods described in [1]-[3]. The results are summarized in Table 1.

Results for the single finger transistor from [1], T_j=188°C, fall within the upper and lower limits, $T_j \in$ [177-236]°C, calculated from the present technique. The large interval found with present technique for the single finger transistor is due to the very high dissipated power in this transistor. This power level is chosen in order to be able to compare with the results in [1]. In normal use the power level of this transistor will be about 25% of the value shown in Table 1, and the estimated interval will be smaller.

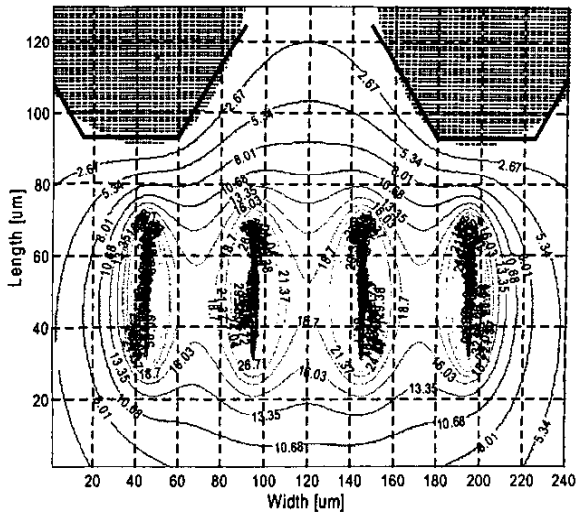

Fig. 1. Contour plot of the temperature increase at the substrate surface of the four-finger transistor.

Results for the four-finger transistor from [1], $T_j \in$ [96.8-105.3]°C, fall within the upper and lower limits, $T_j \in$ [85-106]°C, calculated from the present technique.

Fig. 1 shows the contour plot of the temperature increase at the substrate surface for the four-finger device. The two black dots inside the shaded areas indicate the location of the negative point source in the via-holes. The thick lines at the top of the plot indicate the edge of the physical via-holes, where the temperature increase should be zero. The edges of the shaded areas are where the

TABLE I
Summary of the Results from the Present Technique and the Results from [1]

	1 finger transistor	4 finger transistor				
		Finger no 1	Finger no 2	Finger no 3	Finger no 4	All fingers
Total dissipated power [W]	0.4	0.1	0.1	0.1	0.1	0.4
Power dissipated in the metal [%]	44	22	20	20	22	21
$R_{t,M}$ in the metal [K/W]	864	2615	3093	3093	2615	-
k_{GaAs} at ambient temp. [W/m/K]	46	46	46	46	46	46
k_{GaAs} at junction temp. [W/m/K]	23	31	31	31	31	31
T_j for k_{GaAs} at ambient temp. [°C]	***177***	***83***	***87***	***87***	***83***	***85***
T_j for k_{GaAs} at junction temp. [°C]	***236***	***103***	***109***	***109***	***103***	***106***
Estimated R_{th} [K/W]	380-528	576-778	624-845	624-845	576-778	150-203
T_j from [1] [°C]	***188***	-	-	-	-	***96.8-105.3***

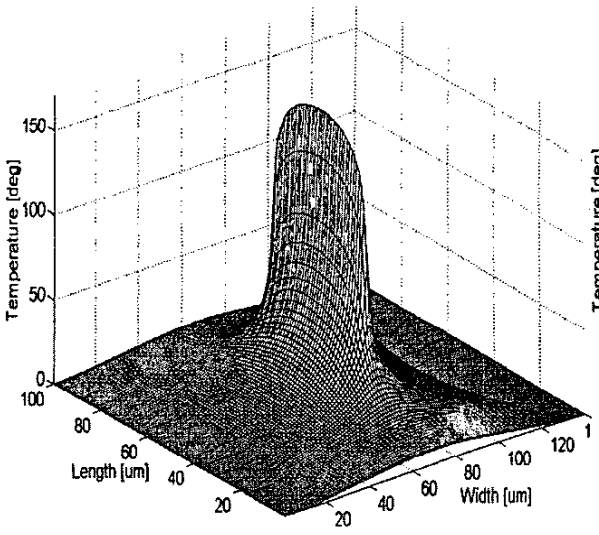

Fig. 2. Plot of the temperature increase at the substrate surface of the one-finger transistor.

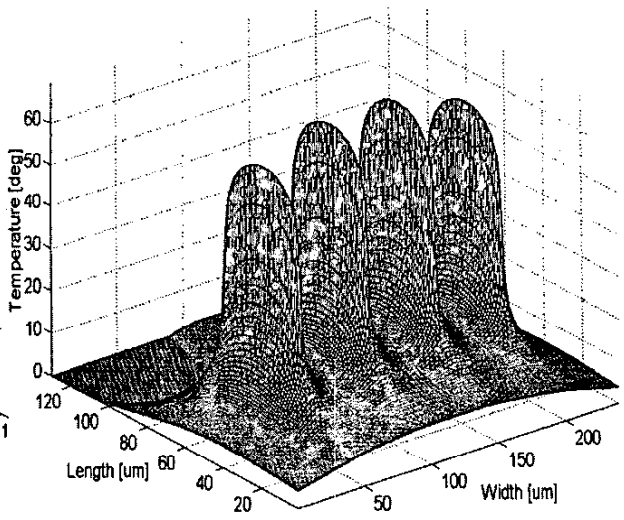

Fig. 3. Plot of the temperature increase at the substrate surface of the four-finger transistor.

temperature increase is calculated to be zero.

The edge of the shaded area follows the thick lines quite well, and confirms that the negative source model gives good match.

Fig. 2 and Fig. 3 show the plots of the calculated temperature increase of the one-finger and the four-finger transistor.

V. Conclusion

In this paper a practical technique of finding a good estimate of the junction temperature and thermal resistance of a GaAs HBT is shown. The present technique uses simple calculations based on the physical dimensions of the transistors and thermal material properties. No specializes software is needed, only a standard mathematical tool like MATLAB. The technique is applied to two different transistors, and compared to results obtained in [1]. The present technique shows good agreement with these results.

The present technique is valid if the metal connected to the emitter is separated from the substrate by a material with very low thermal conduction compared to the thermal conduction of the substrate. This is usually the case in a GaAs HBT.

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